REMARKS

This is a full and timely response to the outstanding FINAL Office Action mailed November 26, 2007. Upon entry of this response, claims 1-6, 13-24, and 32-38 are pending in the present application. Claims 1-6, 13-16, 20-24, and 32-35 are rejected under 35 U.S.C. § 101 allegedly because the claimed invention is directed to non-statutory subject matter. Claims 1-6, 13-15, 20-24, and 32-34 are rejected under 35 U.S.C. §102(b) as allegedly being anticipated by Okumura et al. (U.S. Pat. No. 5,726,923, hereinafter "Okumura"). Furthermore, claims 16-19 and 35-38 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Okumura.

Applicants have analyzed the comments by the Examiner in the Response to Arguments section and respectfully request consideration of the following remarks contained herein intended to clarify the Applicants' arguments.

I. Response to Claim Rejections Under 35 U.S.C. §101

Claims 1-6, 13-16, 20-24, and 32-35 continue to stand rejected under 35 U.S.C. §101 because the claimed invention is allegedly directed to non-statutory subject matter. In particular, the Office Action alleges that the various claims merely disclose steps/components for determining minimum/maximum values without further disclosing a practical/physical application. In the Response to Arguments section, the Office Action asserts that the Applicants do not "appropriately compare" the current application with the cited Okumura patent without providing any explanation. Applicants emphasize in the prior response, Applicants' intention was not to make a direct comparison, but to merely draw attention to the fact that the cited Okumura

patent is itself directed to a minimum/maximum data detector for rapidly detecting the minimum or maximum from a plurality of numeric data.

In an effort to advance prosecution, however, Applicants have amended the claims to overcome the §101 rejection and respectfully request that the §101 rejection be withdrawn. Applicants respectfully submit that these amendments do not necessitate a new search and request entry of the amendments.

II. Response to Claim Rejections Under 35 U.S.C. § 102

It is axiomatic that "[a]nticipation requires the disclosure in a single prior art reference of each element of the claim under consideration." *W. L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1554, 220 USPQ 303, 313 (Fed. Cir. 1983). Therefore, every claimed feature of the claimed invention must be represented in the applied reference to constitute a proper rejection under 35 U.S.C. § 102.

Independent Claim 1

Applicants respectfully submit that independent claim 1 patently defines over Okumura for at least the reason that Okumura fails to disclose, teach or suggest the features emphasized below in claim 1.

Claim 1 recites (emphasis added):

> 1. A processor for reducing the processing effort for determining a minimum value of a plurality of values stored in source registers and determining an index value of a source register having the minimum value, the processor comprising:
> a destination register;
> a first source register storing a first value, wherein the first source register comprises S bits, and wherein the first value comprises N lower bits of the first source register;

a second source register storing a second value, wherein the second source register comprises S bits, and wherein the second value comprises N lower bits of the second source register;

means for comparing the first value stored in the first source register with the second value stored in the second source register;

means for storing the first value in the destination register when the first value is less than or equal to the second value; and

means for concatenating the index value with the second value into a concatenated value and storing the concatenated value in the destination register when the second value is less than the first value, wherein the index value is stored in an upper (S-N) bits of the concatenated value and the second value stored in the N lower bits of the concatenated value.

The Examiner maintains the rejection of claim 1 under Okumura and asserts substantially the same arguments. In the Response to Arguments section, the Examiner asserts that the Okumura reference teaches each of the features in claim 1 with the exception of the index field's location. The Examiner then concludes that "where to place the index field" is merely a design choice. As an initial matter, Applicants point out that as set forth by the Board of Patent Appeals and Interferences, declaring that something is a design choice is a conclusion and not a reason. *Ex Parte Garrett* , 1986, Pat App. Lexus 8 (Bd. Pat. App. Intrf. 1986). Further, the assertion that something is a design choice is insufficient to establish a "suggestion" in the art for the claimed elements. *See e.g., Northern Telecom, Inc. v. Data Point Corp.*, 15 U.S.P.Q. 2d 1321, 1323 (Fed. Cir. 1990). For at least this reason, the rejection should be withdrawn as the Examiner admits that Okumura fails to teach of the one elements recited in claim 1.

Notwithstanding, Applicants submits that the Okumura reference not only fails to teach the limitation regarding the index value (as admitted by the Examiner), Okumura

also fails to teach other limitations recited in claim 1. In particular, Okumura fails to disclose, teach, or suggest the features emphasized above. In alleging that Okumura anticipates claim 1, the Examiner makes the following correlations:

> "first source register" in claim 1 → "specific register 11" in Okumura
> "second source register" in claim 1 → registers 5-6 in Okumura
> "destination register" in claim 1 → "specific register 11" in Okumura

(See Office Action, page 3.) Okumura, however, fails to teach of storing the first value in the destination register when the first value *is less than or equal* to the second value. Reference is made to the related text for steps S7-S9 in FIG. 3 of Okumura:

> Then, in step S7, the contents of the register 5 and those of the specific register 11 are compared . . . If the compared result of step S7 designates that the content of register 5 is less than the content of specific register 11, step S9 is executed.
>
> In step S9, the content of the register 6 and the counted result of the counter 9 are linked . . . and the linked result thereof is stored in the specific register 11. Meanwhile, if the content of the register 5 is judged to be larger than or equal to the content of the specific register 11, step S9 will not be executed.

As set forth above, if the content of the register 5 (allegedly the "second source register" in claim 1) is judged to be larger than or equal to the content of the specific register 11 (allegedly the "first source register" in claim 1), step s9 is simply not executed. Okumura does not teach of storing the first value (specific register 11) in the destination register (specific register 11) when the first value (specific register 11) is less than or equal to the second value (registers 5-6). Claim 1 explicitly recites means for performing a certain function depending on the relationship between the first value and the second value, while Okumura doesn't appear to address this in the cited text/figure. In this respect, Okumura fails to teach of (means for) "storing the first value in the destination register when the first value is less than or equal to the second value."

Accordingly, Applicants respectfully submit that independent claim 1 patently defines over Okumura for at least the reason that Okumura fails to disclose, teach or suggest the highlighted features in claim 1 above. Furthermore, Applicants submit that dependent claims 2-6 are allowable for at least the reason that these claims depend from an allowable independent claim. *See, e.g., In re Fine*, 837 F. 2d 1071 (Fed. Cir. 1988).

Independent Claim 13

Applicants respectfully submit that independent claim 13 patently defines over Okumura for at least the reason that Okumura fails to disclose, teach or suggest the features emphasized below in claim 13.

Claim 13 recites (emphasis added):

> 13. A method for reducing the processing effort for determining a minimum value and a corresponding index value of a plurality of source registers of a processor, the method comprising the steps of:
> for each of the plurality of source registers,
> comparing a value stored in the source register with a value stored in a destination register;
> concatenating the value stored in the source register with an index value associated with the source register and storing the concatenated value in the destination register when the value stored in the source register is less than the value stored in the destination register; and
> ***wherein the destination register initially includes an index value and a value of a first source register of the plurality of source registers***.

In the prior response, Applicants argued that Okumura fails to teach the element, "wherein the destination register *initially* includes an index value and a value *of a first source register* of the plurality of source registers" as Okumura specifically teaches that

"In FIG. 3, when the operation is started, an initial value is stored in the specific register 11 in step S1. The initial value is the maximum value (0x7FFF) is identical to step S31 described in the background art (FIG. 6)." (Col. 4, lines 53-56). The Examiner found this argument to be unpersuasive and in the Response to Arguments section asserts that the limitation (emphasized above) does not require a specific value of the index value and value of first source register. While the recited language in claim 13 does not specify a particular value, the language explicitly recites the limitation wherein the destination register initially includes an index value and a value of a first source register. That is, the destination register is not initialized to simply an "arbitrary number." Okumura teaches of assigning the value 0x7FFF because this represents the maximum value of the numeric data ("the initial value is preferably the maximum value within the expressible scope of the numeric data" -- col. 1, lines 57-59). Okumura fails to teach or suggest that the destination register initially includes an index value and a value of a first source register of the plurality of source registers.

Accordingly, Applicants respectfully submit that independent claim 13 patently defines over Okumura for at least the reason that Okumura fails to disclose, teach or suggest the highlighted features in claim 13 above. Furthermore, Applicants submit that dependent claims 14-16 are allowable for at least the reason that these claims depend from an allowable independent claim.

Independent Claim 20

Applicants respectfully submit that independent claim 20 patently defines over Okumura for at least the reason that Okumura fails to disclose, teach or suggest the features emphasized below in claim 20.

Claim 20 recites (emphasis added):

> 20. A processor for reducing the processing effort for determining a maximum value of a plurality of values stored in source registers and determining an index value of a source register having the maximum value, the processor comprising:
> a destination register;
> a first source register storing a first value;
> a second source register storing a second value;
> means for comparing the first value stored in the first source register with the second value stored in the second source register, ***wherein the first source register and the second source register each include an active status bit to indicate a status of the respective register, and wherein a value of a register having an active status is greater than a value of a register having an inactive status***;
> means for storing the first value in the destination register when the first value is greater than or equal to the second value; and
> means for concatenating the index value with the second value into a concatenated value and storing the concatenated value in the destination register when the second value is greater than the first value.

The Examiner indicates that Applicants' position that Okumura fails to teach the emphasized features above is unpersuasive. In the Response to Arguments section, the Examiner argues that the index field taught by Okumura is equivalent to the "active status bit." In particular, the Examiner submits that "*the index field is either exist or non-exist depending on whether the value is minimum or maximum. Thus, when the index field [sic], it indicates the corresponding data value is maximum or minimum depending on the current comparison.*" (Office Action, page 12). Applicants

respectfully disagree with this reasoning. Okumura does not teach that the index field exists or doesn't exist depending on whether the value is a minimum or maximum. Okumura, in fact, teaches the following in col. 4, lines 22-28:

> The specific register 11 stores new data based on the compared result in the arithmetic logic unit 4. As shown in FIG. 2, the specific register 11 consists of a numeric data field 11a for storing the numeric data, and an index field 11b for storing counted results of the counter 9, namely, the index indicating the input order of the numeric data.

As set forth above, the specific register 11 stores data based on the compared result and consists of both a data field and an index field. Okumura does not teach or suggest that the index field exists or doesn't exist depending on the comparison result. As such, Applicants respectfully maintain that Okumura fails to teach the feature emphasized above in claim 20, and that independent claim 13 patently defines over Okumura for at least this reason. Furthermore, Applicants submit that dependent claims 21-24 are allowable for at least the reason that these claims depend from an allowable independent claim.

Independent Claim 32

Applicants respectfully submit that independent claim 32 patently defines over Okumura for at least the reason that Okumura fails to disclose, teach or suggest the features emphasized below in claim 32.

Claim 32 recites (emphasis added):

> 32. A method for reducing the processing effort for determining a maximum value and a corresponding index value of a plurality of source registers of a processor, the method comprising the steps of:
> for each of the plurality of source registers,

> comparing a value stored in the source register with a value stored in a destination register;
>
> concatenating the value stored in the source register with an index value associated with the source register and storing the concatenated value in the destination register when the value stored in the source register is greater than the value stored in the destination register; and
>
> ***wherein the destination register initially includes an index value and a value of a first source register of the plurality of source registers***.

In the prior response, Applicants argued that Okumura fails to teach the element, "wherein the destination register *initially* includes an index value and a value *of a first source register* of the plurality of source registers" as Okumura specifically teaches that "In FIG. 3, when the operation is started, an initial value is stored in the specific register 11 in step S1. The initial value is the maximum value (0x7FFF) is identical to step S31 described in the background art (FIG. 6)." (Col. 4, lines 53-56). The Examiner found this argument to be unpersuasive and in the Response to Arguments section relies on the same reasoning used to address claim 13. That is, the Examiner argues that the limitation (emphasized above) does not require a specific value of the index value and value of first source register.

Applicants submits that while the recited language in claim 32 does not specify a particular value, the language explicitly recites the limitation wherein the destination register initially includes an index value and a value of a first source register and is not initialized to simply an "arbitrary number." Okumura teaches of assigning the value 0x7FFF because this represents the maximum value of the numeric data ("the initial value is preferably the maximum value within the expressible scope of the numeric data" -- col. 1, lines 57-59). Okumura fails to teach or suggest that the destination

register initially includes an index value and a value of a first source register of the plurality of source registers.

Accordingly, Applicants respectfully submit that independent claim 32 patently defines over Okumura for at least the reason that Okumura fails to disclose, teach or suggest the highlighted features in claim 32 above. Furthermore, Applicants submit that dependent claims 33-35 are allowable for at least the reason that these claims depend from an allowable independent claim.

III. Response to Claim Rejections Under 35 U.S.C. § 103

The USPTO has the burden under section 103 to establish a *prima facie* case of obviousness according to the factual inquiries expressed in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966). The four factual inquires, also expressed in MPEP §2141, are as follows:

(A) Determining the scope and contents of the prior art;

(B) Ascertaining the differences between the prior art and the claims in issue;

(C) Resolving the level of ordinary skill in the pertinent art; and

(D) Evaluating evidence of secondary considerations.

For at least the reasons set forth below, Applicants traverse the §103 rejections set forth in the Office Action.

Independent Claim 17

Applicants respectfully submit that independent claim 17 patently defines over Okumura for at least the reason that Okumura fails to disclose, teach or suggest the features emphasized below in claim 17.

Claim 17 recites (emphasis added):

> 17. A customer premise equipment (CPE) comprising:
> a network interface operably connected to a first network segment;
> a network interface operably connected to a second network segment; and
> a processor operably connected to the network interfaces and being adapted to:
> ***compare a first value stored in a first source register of the processor with a second value stored in a second source register of the processor;***
> ***store the first value in a first destination register of the processor when the first value is less than or equal to the second value***; and
> ***store the second value in the first destination register of the processor and an index value in a second destination register of the processor when the second value is less than the first value, the index value representing the second source register***.

In the Response to Arguments section, the Examiner rejects the Applicants' argument that Okumura fails to teach of storing the second value in the first destination register of the processor and an index value in a second destination register of the processor. The Examiner asserts that FIG. 2 of Okumura "*clearly discloses the numeric field and the index field*" and further asserts that "*the result of the comparison is saved/stored in the numeric data field called the first destination register. . .*" Okumura, however, makes no reference to a "destination register" much less to a "first destination register" and a "second destination register." Applicants respectfully maintain that Okumura fails to teach this feature.

Applicants also submit that Okumura fails to disclose a processor adapted to 1) store the first value in a first destination register of the processor when the first value is less than or equal to the second value; and 2) store the second value in the first destination register of the processor and an index value in a second destination register

of the processor when the second value is less than the first value. That is, based on the comparison result of the first source register and second source register, the processor performs a certain action. If the first value is less than or equal to the second value, the processor stores the first value in a first destination value. If the second value is less than the first value, the processor stores the second value in the first destination register of the processor and an index value in a second destination register.

In the rejection, the Examiner alleges that Okumura teaches these operations in FIG. 3. Specifically, the Examiner makes the following correlations:

"store the first value in a first destination register of the processor when the first value is less than or equal to the second value" in claim 17 → Okumura reference: "e.g., path when specific register 11 is less than register 5 in Figure 3"

"store the second value in the first destination register of the processor and an index value in a second destination register of the processor when the second value is less than the first value" in claim 17 → Okumura reference: "e.g., step S9 in Figure 3"

According to FIG. 3 of Okumura, step s9 is performed if register 5 is less than specific register 11. However, when specific register 11 is less than register 5, then step s9 is simply not executed. Okumura fails to teach of storing the first value in a first destination register. (*See* FIG. 3, Okumura.)

Accordingly, Applicants respectfully submit that independent claim 17 patently defines over Okumura for at least the reason that Okumura fails to disclose, teach or suggest the highlighted features in claim 17 above. Furthermore, Applicants submit that dependent claims 18-19 are allowable for at least the reason that these claims depend from an allowable independent claim.

Independent Claim 36

Applicants respectfully submit that independent claim 36 patently defines over Okumura for at least the reason that Okumura fails to disclose, teach or suggest the features emphasized below in claim 36.

Claim 36 recites (emphasis added):

> 36. A customer premise equipment (CPE) comprising:
> a network interface operably connected to a first network segment;
> a network interface operably connected to a second network segment; and
> a processor operably connected to the network interfaces and being adapted to:
> ***compare a first value stored in a first source register of the processor with a second value stored in a second source register of the processor;***
> ***store the first value in a first destination register of the processor when the first value is greater than or equal to the second value; and***
> ***store the second value in the first destination register of the processor and an index value in a second destination register of the processor when the second value is greater than the first value, the index value representing the second source register.***

In the Response to Arguments section, the Examiner rejects the Applicants' argument. Okumura, however, makes no reference to a "destination register" much less to a "first destination register" and a "second destination register." Applicants respectfully maintain that Okumura fails to teach this feature.

Applicants also submit that Okumura fails to teach of a processor adapted to 1) store the first value in a first destination register of the processor when the first value is greater than or equal to the second value; and 2) store the second value in the first destination register of the processor and an index value in a second destination register of the processor when the second value is greater than the first value. In the related

text for FIG. 3, Okumura teaches that step s9 is either executed or not executed, depending on the comparison result between register 5 and specific register 11. This is not equivalent to the features emphasize above in claim 36.

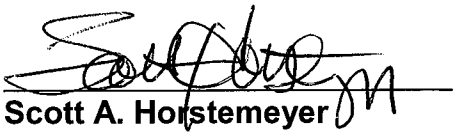
Accordingly, Applicants respectfully submit that independent claim 36 patently defines over Okumura for at least the reason that Okumura fails to disclose, teach or suggest the highlighted features in claim 36 above. Furthermore, Applicants submit that dependent claims 37-38 are allowable for at least the reason that these claims depend from an allowable independent claim.

CONCLUSION

Applicants respectfully submit that all pending claims are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephone conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,



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